A Comparative Review on ALU using CMOS and GDI techniques for Power Dissipation and Propagation Delay

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ABSTRACT

Arithmetic and Logic Circuits are to be designed with less power, compact size, less propagation delay in this fast growing era of technology. Arithmetic operations are indispensable and the basic functions for any high speed low power applications like digital signal processing, microprocessors, image processing, etc. Consumption of power is the major issue in designing these circuits. Also the number of transistors required is also the one of the issues in designing the circuits. To minimize the transistors required in designing the circuits and to reduce the power consumption of the circuits, the authors have referred some techniques to overcome these problems in this paper. By reviewing all these techniques, the authors try to implement the GDI technique to reduce the power consumption and transistors count or the area required to design the circuits.

I. INTRODUCTION

Reducing power losses in VLSI circuits is becoming one of the most significant challenges in the semiconductor industry [1,2]. Performance optimization techniques are applied to all semiconductor design levels. Advanced processors offer numerous architectural improvements, such as branch forecasting, software hardware co-optimization, and the use of multiple cores in a single processor [3]. Portability requirements for laptops and other portable devices significantly limit size and power consumption. Although battery technology is constantly improving and processors and displays are improving rapidly in terms of power consumption, battery life and weight are factors that have a significant impact on the way laptops can be used for [4]. These devices often require real-time processing functions and therefore require high throughput. Energy consumption becomes the limiting factor for the range of functions of these devices. The wider and continuous use of network services will only exaggerate this problem because communication consumes a relatively high amount of energy. The gradual downsizing of the technology has led to the use of lower supply voltages for CMOS circuits, which affects lower threshold voltages to improve performance. As the channel length decreases for future technology generations, the threshold voltage and gate oxide thickness are also reduced to keep pace with performance [5]. A lower threshold voltage leads to an exponential increase in the leakage current because the transistors cannot be completely turned off. In a CMOS circuit, total power loss includes dynamic and static components. The components of static power loss are losses below the threshold, junction losses, gate oxide losses, network-induced drainage losses and breakage losses. This applies to directly battery-powered portable devices such as cell phones and PDAs, as they have a long service life. Different techniques used to effectively minimize this power loss. Stack Keeper is a technique for reducing losses. We analyze that the technique for reducing low power leakage losses is the gate diffusion input. Use only three input names N, P and G in the grid transmission input technology. This connector is used to implement a simple function. Here, we applied this technique to a 1-bit 2x1MUX, 4X1MUX, 16X1MUX and ALU [6].

Multiplexers are combinatorial circuits in which the number of signals is multiplexed and combined and flows through the comment device. In other words, an electronic multiplexer allows multiple signals to share a device or resource. An electronic multiplexer can be considered as a switch with multiple inputs and one output. This arithmetic logical unit is produced using this multiplexer.

An arithmetic and logic unit or ALU performs many different arithmetic and logic operations. ALU is the "heart" of a processor: it could be said that everything else in the CPU is used to support ALU.[7] The logical arithmetic unit (ALU) is the structure of the computer, the

device that performs arithmetic operations such as addition and subtraction or logical operations such as AND and OR. This section creates an ALU from four hardware components (AND and OR gates, inverters and multiplexers) and shows how combinational logic works. Logical operations are the simplest since they are directly mapped to hardware components. The 1-bit logical unit for AND and OR is similar. The multiplexer on the right then selects an AND b or an OR b depending on whether the operating value is 0 or 1. The multiplexer control and output lines indicate names that reflect the function of the ALU [8].

II. LITERATURE REVIEW

Kaushik Roy et. al. [1] This results in a high leakage current in the deep sub-micrometric range and contributes significantly to the power loss of the CMOS circuits since the threshold voltage, channel length and gate oxide thickness are reduced. Therefore, the identification and modeling of various components of the leakage current are of great importance for estimating and reducing the leakage current, particularly in low energy consumption applications.

Afshin Abdollahi et al.[2] they have reduced the leakage current in the sequential circuits by modifying the scan chains wherein the control of the input vector is an effective technique for reducing the leakage current of the combined VLSI circuits when these circuits are in standby mode. This article proposes a design technique for applying the minimum leakage current input to a sequential circuit. Our method uses the scan chain integrated into a VLSI circuit to control it with the minimum dispersion vector when it goes into standby mode.

Afshin Abdollahi, Farzan Fallah et al. [3] this paper presented are the offer a reduction of the leakage current in the CMOS-VLSI circuits thanks to the input vector control, in which the first part of this work describes two execution mechanisms to reduce the leakage current of a CMOS circuit. In either case, the system or environment should generate a "sleep" signal which can be used to indicate that the circuit is in sleep mode. In the first method, the "sleep" signal is used to move a new set of external inputs and pre-selected internal signals in the circuit in order to define the logical values of all the internal signals so that the sum of the leakage current is a minimized circuit.

III. VLSI DESIGN FLOW CHART

The design process begins with the behavior of the target circuit. The corresponding circuit architecture is first defined and mapped. The next design development in the behavioral domain defines those that will be structurally implemented with functional modules such as multiplexers and arithmetic logical units (ALU).

These modules are then positioned geometrically on the chip surface using CAD tools for the automatic positioning of the modules followed by routing, in order to minimize the interconnection area and signal delays. The third evolution begins with a description of the behavioral module. The individual modules are then implemented with a circuit. At this point, the circuit is described in terms of logic gates, which can be positioned and interconnected using a cell positioning and routing program.
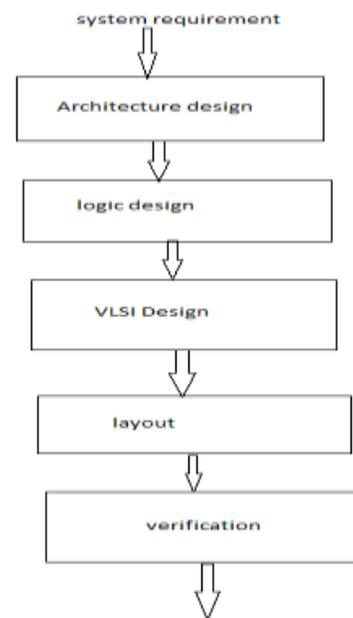

Figure 1: VLSI Design flow chart

IV. BASIC GDI FUNCTIONS

The GDI technology is based on the simple cell as shown in Fig. 1. The basic cell reminds of the CMOS inverter, but there are some important differences.

1) The GDI cell has three inputs: (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

2) Both bulks of NMOS and PMOS are connected to N or P (respectively), so it is biased at contrast with a CMOS inverter.
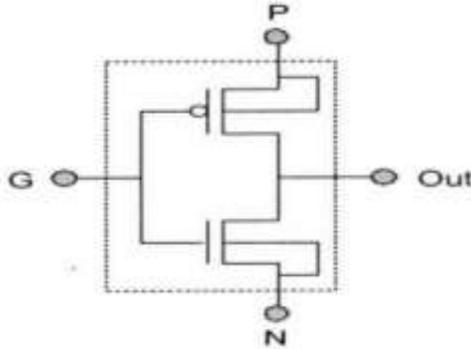

Figure 2 GDI basic cell

It must be noticed that not all of the functions are possible in standard p-well CMOS process but they can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies.

V. ALU

ALU is a component of several circuits. When designing the ALU, we follow the "divide and conquer" principle to use a modular design made up of smaller and more manageable blocks, some of which can be reused.

The ALU is part of a microprocessor or microcontroller which processes all Boolean and mathematical operations. It is a basic element of a computer's central processing unit. The microprocessor has traditionally been designed around these essential units such as the decoding unit, the ALU (arithmetic and logic unit), time control and the control unit. The arithmetic and logically linked operations in the microprocessor are performed by the ALU. The content of many different circuits, arranged on a single chip, forms an integrated circuit. With the introduction of the integrated circuit, all peripherals and the microprocessor have been combined into a single device. This led to the development of a microcontroller. A microcontroller differs from the microprocessor in many ways. The most important aspect is functionality.
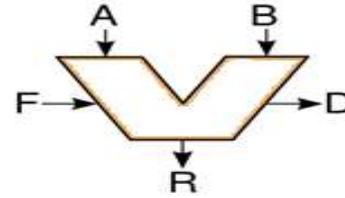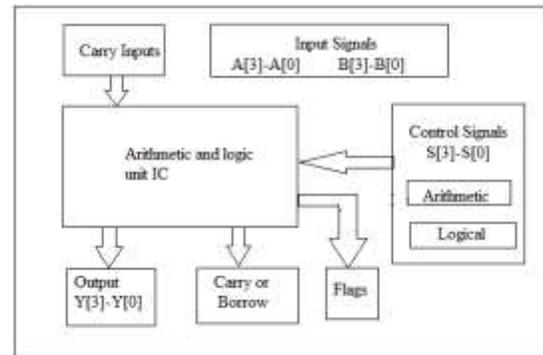

Figure 3: Symbol for an ALU

Figure 4: Block Diagram of ALU

VI. MULTIPLEXER

A multiplexer (or MUX) is a device that selects one of the analog or digital input signals and transmits the selected input on a single line.

A multiplexer with 2n inputs has n selection lines, which are used to select the input line to be sent to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a specified time and bandwidth. A multiplexer is also called a data selector.

VII. CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power

consumption. In this paper we presented a study of novel low power and low transistor count 4 bit ALU and compared its performance for power consumption, area and delay. Analysis and simulation studies were performed on 4bit ALU using GDI Technique. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, GDI techniques.

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